# High Reliable Design and Implementation of 5G NR PUSCH Equalization on FPGA


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## Background & Motivation

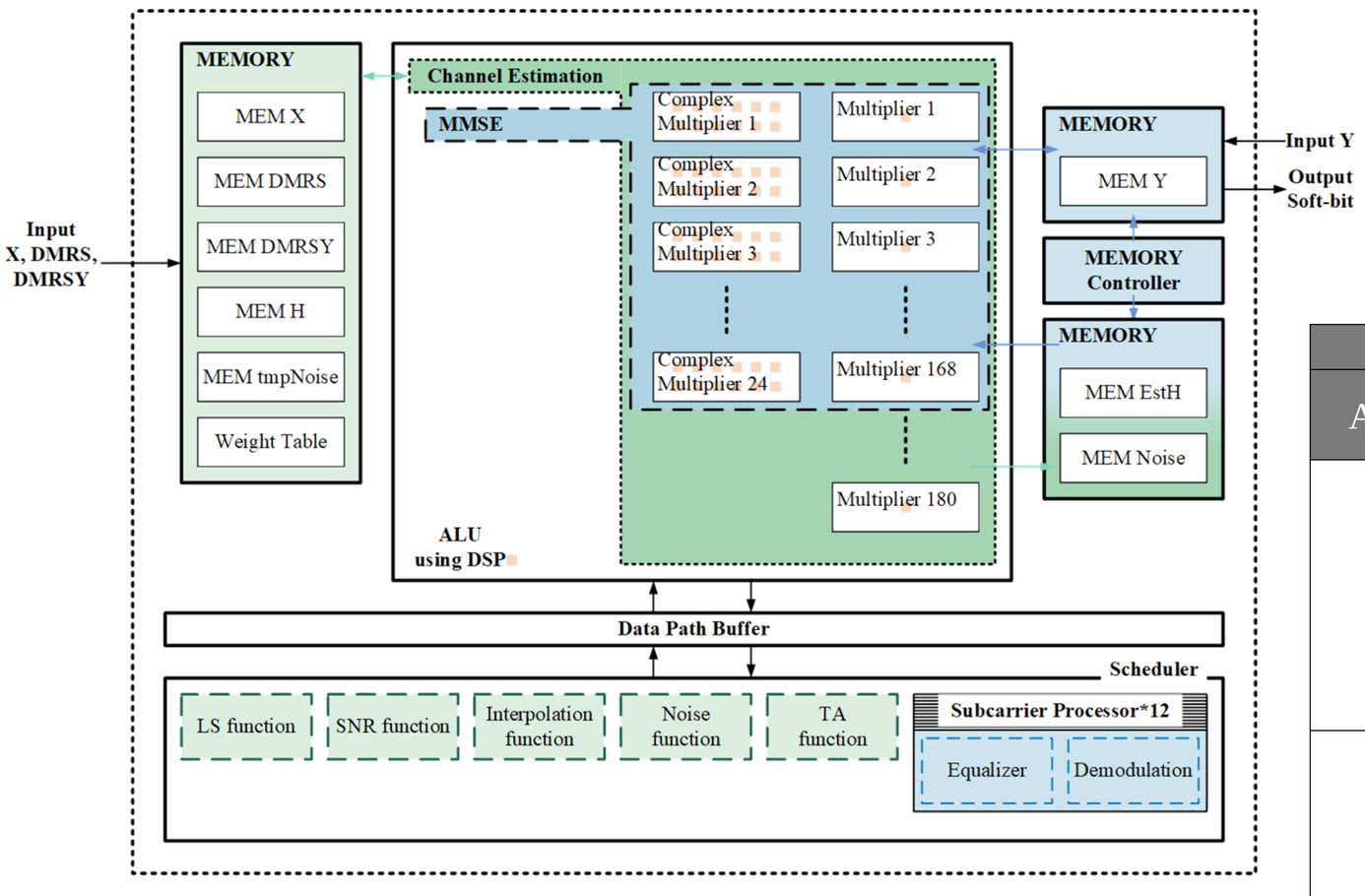
- In the era in which the network is developing at a high speed, the support of a large number of semiconductor chips is required.
- However, it takes too long and the cost is too high for the design and production of semiconductor chips
- Use Field Programmable Gate Array with unique computing capabilities to accelerate the base station operation for the first layer in the wireless communication network: the physical layer

## Contribution

- Design and implement MMSE on FPGA
- Use Cholesky decomposition for matrix inverse in equalization
- smaller divider/adder：64-bit(traditional) → 32-bit
- Use pipelined multiplier/divider/adder
- reduce clock cycle time to 5ns
- Same execution time for single user case and multi-user case (same total RB & DMRS num)
- Execution time for 2T2R worst case：82.8μs

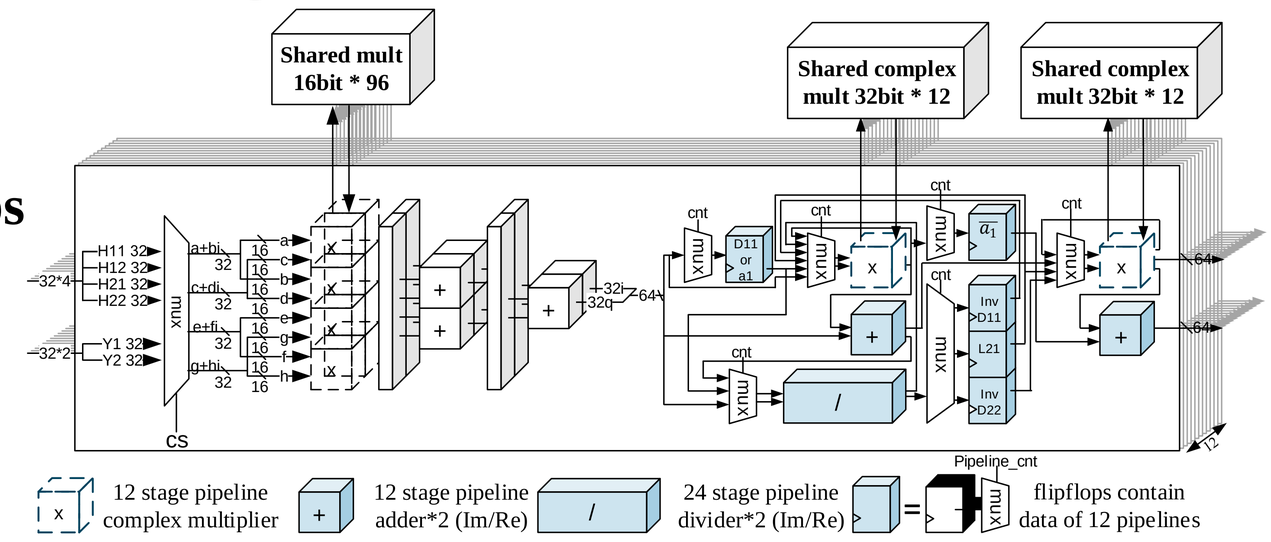
## Integrated with Channel Estimation

- Integration reduce the usage of DSP



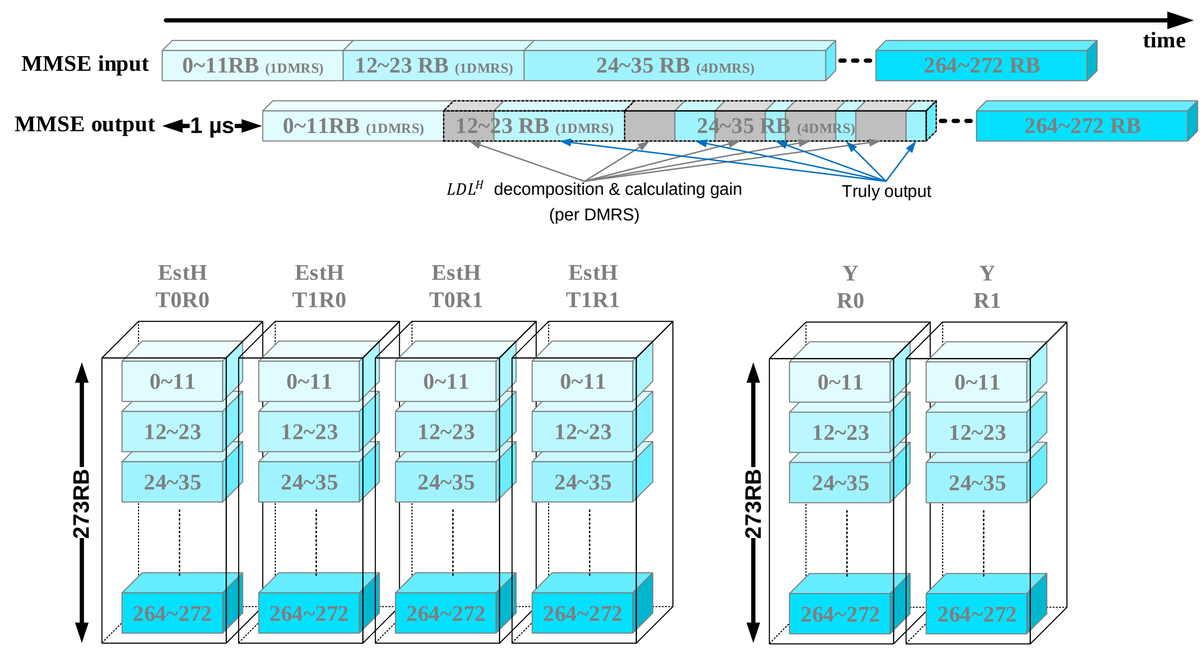

## Hardware Architecture

- Fully pipelined equalization design to calculated each RB parallel

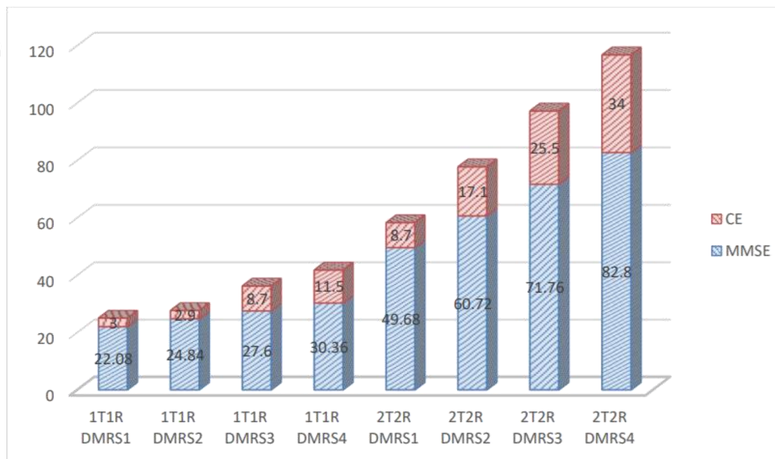



## Execution Timeline

- Process 12RB once a time




## Performance




| Scenario | | Total time($\mu s$) | CE | | MMSE | |
|---|---|---|---|---|---|---|
| Antenna | # of DMRS | | Time($\mu s$) | % | Time($\mu s$) | % |
| 1T1R | 1 | 25.1 | 3 | 12% | 22.1 | 88% |
| | 2 | 30.7 | 5.9 | 19% | 24.8 | 81% |
| | 3 | 36.3 | 8.7 | 24% | 27.6 | 76% |
| | 4 | 41.9 | 11.5 | 27% | 30.4 | 73% |
| 2T2R | 1 | 58.7 | 8.7 | 15% | 50.0 | 85% |
| | 2 | 77.8 | 17.1 | 22% | 60.7 | 78% |
| | 3 | 97.3 | 25.5 | 26% | 71.8 | 74% |
| | 4 | 116.8 | 34 | 29% | 82.8 | 71% |