Improving TLC NAND Flash Read Performance Using Adaptive Bit Coding

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Abstract

NAND-based Solid-State Drive (SSD) has become the mainstream storage solution as it provides high-performance and non-volatile data storage. With the adoption of high cell-bit density, the error margin between adjacent threshold voltage states becomes very narrow and thus erroneous bit values quickly emerge as retention time increases. Modern SSDs employ Low-Density Parity-Check (LDPC) for error correction, but it utilizes multiple voltage sensing operations to determine the probability-based bit input and the time overhead of voltage sensing is high. In this study, we identify that the flash read latency is highly subject to the bit coding method, and adaptive switching between different coding methods offers an opportunity for optimizing the flash read latency according to how frequent data is read by the host. Specifically, we propose using 2-3-2 coding as default and migrating frequently-read data to a fast page using 1-2-4 coding. Our experimental results show that our design reduces the read latency by 50%, 35%, 23% compared against 1-2-4 baseline, 2-3-2 baseline, 1-2-4 FastRead, respectively.

Motivation

Read latency = Total Vth sensing time + Transfer time + LDPC decoding time

2-3-2 Coding: Pros and Cons

- When retention time is not short (>= 1 mo)
- Pros: average read latency (LSB/CSB/MSB) is better
- Cons: CSB/MSB pages are relatively slow

type	124-gray coding			232-gray coding		
retention	LSB	CSB	MSB	LSB	CSB	MSB
1 day	66	104	180	104	142	104
1 month	229	305	1075	305	435	335
3 months	229	324	1652	305	782	587
6 months	229	356	1705	305	847	771

=2290 =1923 average latency is shorter!

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1-2-4 Coding: Pros and Cons

- When retention time is not short (>= 1 mo)
- Pros: LSB/CSB pages are relatively fast
- Cons: MSB page is very slow

type	124-gray coding			232-gray coding		
retention	LSB	CSB	MSB	LSB	CSB	MSB
1 day	66	104	180	104	142	104
1 month	229	305	1075	305	435	335
3 months	229	324	1652	305	782	587
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fast page very slow page slow page

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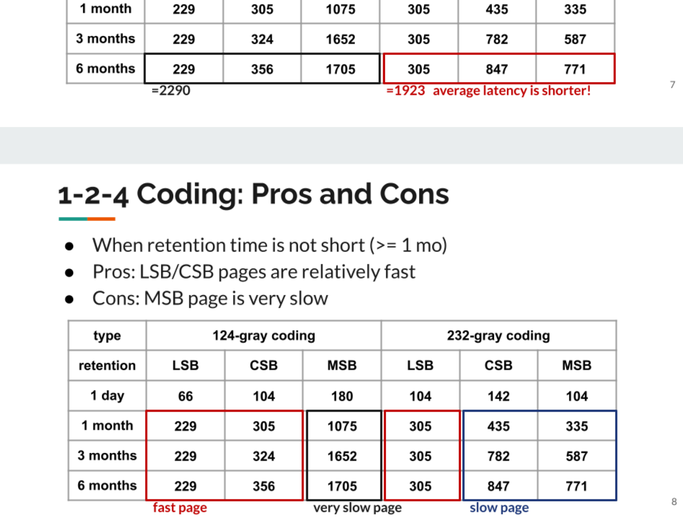
Design Overview

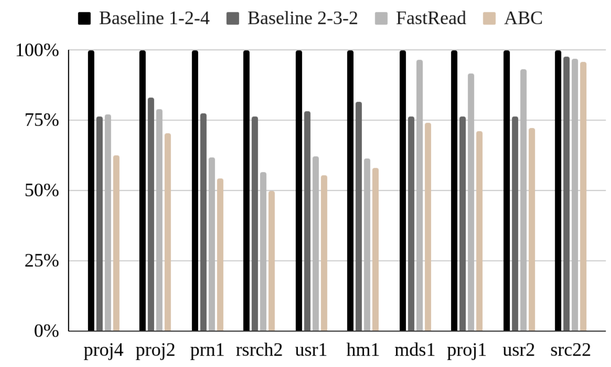
Three new components in FTL

- Read-Hot Data Identifier
- Code Type Manager
- Page Migrator

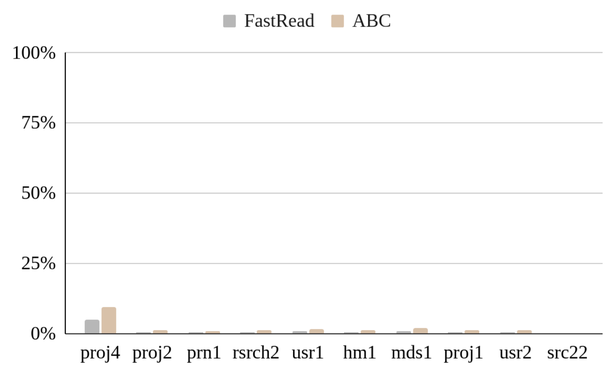


Experimental Results

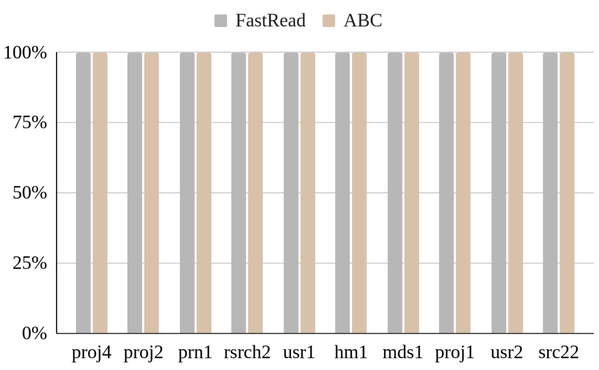
A. Read latency



B. Migration cost



C. Efficacy of migration



Conclusion

In modern SSDs, LDPC provides strong error correction capability. It increases sensing level to decode the overlapping Vths caused by noises accurately. The more sensing levels it uses, the longer the decoding delay. However, the read latency varies according to all pages with gray coding schemes and retention time. The gray coding affects the read latency in two ways. 1) the number of reference voltages for reading a page. 2) retention errors cause the unbalanced rBER between Vth states, especially severe at high voltage states. In this study, we observed that the tradeoff between 1-2-4 coding and 2-3-2 coding highly depends on the sensing levels and bit-error rate distribution. Hence, we can exploit the fast pages in 1-2-4 coding and an overall average latency of 2-3-2 coding. We propose an adaptive bit coding approach to reduce the read latency. The strategy is based on using 2-3-2 coding as default and migrating read-hot data to a fast page using 1-2-4 coding, which takes advantage of two coding types. Experimental results demonstrated that our adaptive bit coding approach could improve the read performance of read-oriented workloads up to 50\%, 35\%, 23\% compared with the 1-2-4 baseline, 2-3-2 baseline, 1-2-4 FastRead, respectively. The overhead is a small proportion of total writes, and most of the migrations are effective.